UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,048	01/26/2004	Raminda Udaya Madurawe		7613

33380 7590 06/30/2004

RAMINDA U. MADURAWE
882 LOUISE DRIVE
SUNNYVALE, CA 94087

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,048	MADURAWE, RAMINDA UDAYA	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 20* is/are rejected.

7)☒ Claim(s) *17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 01/26/2004 is acceptable.

Drawings

2. Figures 1A, 1B, 2A, 2B, 3A, 3B, and 4 through 7 should be designated by a legend such as – Prior Art –, or – Background Art –, or – Related Art – in order to clarify what is applicants' invention. (See MPEP § 608.02(g)).

Correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 13-14, 16-18, 1-3, 6-11,

and 19 of copending Application No. 10/413,810. Although the conflicting claims are not identical, they are not patentably distinct from each other.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-5** are rejected under 35 U.S.C. 102(b) as being anticipated by Plus et al. U.S. Patent 4,872,141 (the '141 patent).

The '141 patent discloses in Figures 1-3 and respective portions of the specification a method of forming a semiconductor latch for integrated circuits as claimed.

Referring to **claim 1**, the '141 patent discloses a method of forming a semiconductor latch for integrated circuits, said latch adapted to receive a first supply voltage VDD and a second supply voltage (Ground) substantially at a lower voltage level than said first supply voltage, the method comprised of :

fabricating a first and a second conducting path of a first inverter 12, defined by transistors 16 and 30 of Figure 1, in a first semiconductor layer 52 (Fig. 2), said first conducting path coupled between said first supply voltage and an output, said second conducting path coupled between said second supply voltage and said output;

depositing an isolation layer 64 above said first inverter; and

fabricating a first and a second conducting path of a second inverter 14, defined by transistors 16a and 30a of Figure 1 in a second semiconductor layer 54 (Fig. 2), said first conducting path coupled between said first supply voltage and an output, said second conducting path coupled between said second supply voltage and said output.

Note that although Figures 2 and 3 depicts only the steps for transistors 30 and 30a, column 2, last paragraph, details the steps for transistors 16 and 16a.

Referring to **claim 2**, the '141 patent further discloses that said first semiconductor layer is one of substrate Silicon, amorphous Silicon, poly-crystalline Silicon, laser annealed poly-crystalline Silicon, compound semiconductor material, Silicon on insulator, and any other semiconductor material.

The materials recited in **claims 3 and 4**, just as the materials recited in claim 2, oxide and silicon, are available and known in the art.

Referring to **claim 5**, as noted above, although Figures 2 and 3 do not show transistors 16 and 16a, and in effect do not show the conductions paths of transistor 16a, transistor 16a and its conduction paths together with transistor 30a and its conduction paths constitute the second inverter 14, and these conduction paths are fabricated on a single geometry of said second semiconductor layer 54.

6. **Claims 6-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller the '141 patent for being obvious.

Referring to **claim 6**, the '141 patent discloses a method as claimed and as detailed above, including forming a respective gate for first inverter 12 and second inverter 14 for respectively modulating said respective first and second conducting paths of said first inverter and said second inverter to couple either said first supply voltage or said second supply voltage to said first inverter output or to said second inverter output, but fails to disclose that the gate of the first inverter or the gate of the second inverter is a common gate. However, it is known in the semiconductor static random access memory art, just as admitted by Applicant in Figures 1 to 7 of the conventional SRAM, that a common gate or two gates electrically connected together are just various methods one of ordinary skill in the art would find obvious for forming a gate for an SRAM.

The pull-up and pull-down transistors as recited in **claims 7-8** are inherent in the '141 patent' semiconductor SRAM.

Referring to **claims 9, t**he '141 patent further discloses forming a pass-gate transistor 42 having a conducting path coupled between gate of inverter 14 and a data line 44, and forming a

gate 46 above said conducting path, said gate coupled to a row line 48, said gate at a first voltage level substantially coupling said data line to said common gate of first inverter, said gate at a second voltage level substantially de-coupling said data line from said common gate of first inverter. However, the reference fails to explicitly show how to fabricate the pass-gate transistor 42 in relation to inverter 14, thus in effect is quiet about the location of the conducting path of the pass-gate transistor 42; i.e., the reference fails to disclose that the conducting path of the pass-gate transistor 42 is formed in the same semiconductor layer in which inverter 14 is fabricated. Nevertheless, forming the conducting path of the pass-gate transistor 42 in the same semiconductor layer in which inverter 14 is fabricated would have been obvious because the '141 patent has also failed to show otherwise, i.e., forming the conducting path of the pass-gate transistor 42 in a semiconductor layer different from the layer that inverter 14 is fabricated. Forming the conducting path of the pass-gate transistor 42 in a semiconductor layer different from the layer that inverter 14 is fabricated would have required more steps and more IC "real estate", characteristics that one of ordinary skill in the art would not contemplate.

Referring to **claim 10**, forming a single pass-gate transistor for SRAM, as disclosed by the '141 patent, or forming a dual pass-gate transistor for SRAM, as recited by claim 10, are just various ways one of ordinary skill in the art would find obvious for forming pass-gate transistors for an SRAM.

Referring to **claim 11**, as noted above, although Figures 2 and 3 do not show transistors 16 and 16a, and in effect do not show the conductions paths of transistor 16a, transistor 16a and its conduction paths together with transistor 30a and its conduction paths constitute the second inverter 14, and these conduction paths are fabricated on a single geometry of said second

semiconductor layer 54. And also as note above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the pass-gate transistor 42 in the same semiconductor layer in which inverter 14 is fabricated, and therefore it would have been obvious to form the conducting path of said pass-gate transistor, together with the conducting path of the second inverter, on a single geometry of said second semiconductor layer.

7. **Claims 12-16 and 20** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bertin et al. U.S. Patent 6,137,129 (the '129 patent).

The '129 patent discloses in the figures, particularly Figure 16, and respective portions of the specification a method substantially as claimed. The '129 patent discloses a semiconductor module 272 used to construct logic circuits ("pass-gate wafer" or a logic-circuit layer) and a semiconductor layer for forming a bi-stable latch ("latch wafer" 270, or a memory layer). However, it appears that the logic-circuit layer is formed above the memory layer instead of being below the memory layer as claimed. Except for this difference, the structure and processes of Figure 16 are the same as those claimed.

In particular and with reference to **claim 20**, the '129 patent disclose a method of fabricating a semiconductor latch for an integrated circuit, comprised of:

forming two inverters, said inverters cross-coupled to form a bi-stable latch (Figure 16 and Abstract); and

supplying each of said inverters with a first supply voltage Vps and a second supply voltage Gnd, said second supply voltage substantially lower than said first supply voltage level,

and fabricating at least one of said inverters in a semiconductor thin film module 270, said module layers deposited substantially *below* a semiconductor module 272 used to construct logic circuits.

As noted above, semiconductor thin film module 270 is below semiconductor module 272 instead of being above as claimed (and therefore semiconductor module 272 is not really a substrate). However, both the specification of the present invention and that of the '129 patent have not convinced the examiner of any substantial difference between the two structures and therefore change from one structure to the other, e.g., forming semiconductor thin film module 270, said module layers deposited substantially *above* a semiconductor substrate module 272 used to construct logic circuits, would have been obvious.

Note also that although the '129 patent does not explicitly disclose that module 270 is thin film, it would appear that module 270 is thin film because only layer 312 (Fig. 17 and column 10, lines 24-25 and claim 10) is addressed as being bulk. Since module 270 is not bulk, it appears that it is thin film.

In a similar reasoning, **claim 12** is obvious over:

a method of forming a semiconductor latch for integrated circuits, said latch adapted to receive a first supply voltage Vps and a second supply voltage Gnd substantially at a lower voltage level than said first supply voltage, the method comprising:

depositing an isolation layer TEOS 282 *below* a first module layer 272, said module comprising a semiconductor (substrate) layer used to fabricate logic transistors ("pass-gate" transistors); and

depositing a semiconductor thin film layer; and fabricating a first and a second conducting path of a first inverter (defined by structure 100 or two of the four vertical columns in layer 270, Figures 1, 2, and 16) in said semiconductor thin film layer, said first conducting path coupled between said first supply voltage and a first output, said second conducting path coupled between said second supply voltage and said first output; and

fabricating a first and a second conducting path of a second inverter (defined by structure 100 or the other two of the four vertical columns in layer 270, Figures 1, 2, and 16) in said semiconductor thin film layer, said first conducting path coupled between said first supply voltage and a second output, said second conducting path coupled between said second supply voltage and said second output.

As noted above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to change *below* to *above*.

The materials of **claims 13 and 14** are available and known in the art (the isolation layer is one of oxide, the semiconductor thin film layer is any semiconductor material).

Referring to **claim 15**, the '129 patent further discloses that first and second conducting paths of said first and second inverters are fabricated on a single geometry of said semiconductor thin film layer.

Regarding **claim 16**, the '129 patent further discloses, in Figures 1, 2, and 16, forming a common gate (no number, but note that "each device's source or drain is the gate of the other device", column 2, line 26) for said first inverter, said gate modulating said first and second conducting paths of said first inverter to couple either said first supply voltage or said second supply voltage to said first inverter output; and

forming a common gate (no number, but note that "each device's source or drain is the gate of the other device", column 2, line 26) for said second inverter, said gate modulating said first and second, conducting paths of said second inverter to couple either said first supply voltage or said second supply voltage to said second inverter output; and coupling said first output of first inverter to said common gate of second inverter, and coupling said second output of second inverter to said common gate of first inverter.

Allowable Subject Matter

8. **Claims 17-19** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten to overcome the objection noted above.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a method of forming a semiconductor latch having all exclusive limitations as recited in claims 12/17 (claims 12 and 17) and claims 12/18, comprising forming a first inverter, a second inverter, and logic transistors as detailed in claim 12, characterized in depositing a dielectric layer on said semiconductor thin film layer and forming gate dielectric regions above channel regions for said pull-up and pull-down transistors or forming a pass-gate transistor comprising forming a conducting path in said semiconductor thin film layer and forming a gate above said conducing path.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
June 26, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800